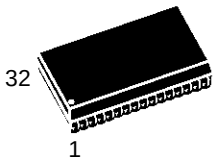
SGS-THOMSON MICROELECTRONICS

M628128

1 Megabit (128K x 8) VERY FAST SRAM WITH OUTPUT ENABLE

- 128K x 8 VERY FAST SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 15, 20ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- JEDEC PLASTIC SOJ, 400 mil PACKAGE



SOJ32 (E)
400 mils

DESCRIPTION

The M628128 is a 1 Megabit (1,048,576 bit) Fast CMOS SRAM, organized as 131,072 words by 8 bits. It is fabricated using SGS-THOMSON's Advanced, low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ± 10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

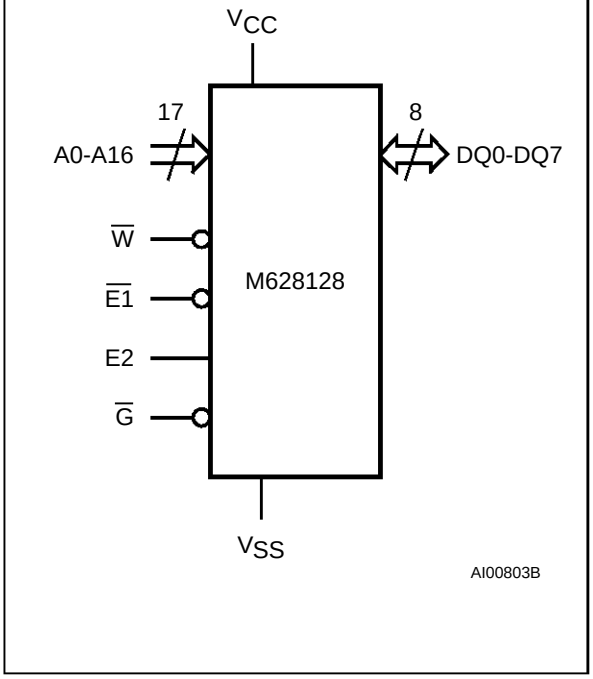


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 7	V
I_O (3)	Output Current	20	mA
P_D	Power Dissipation	1	W

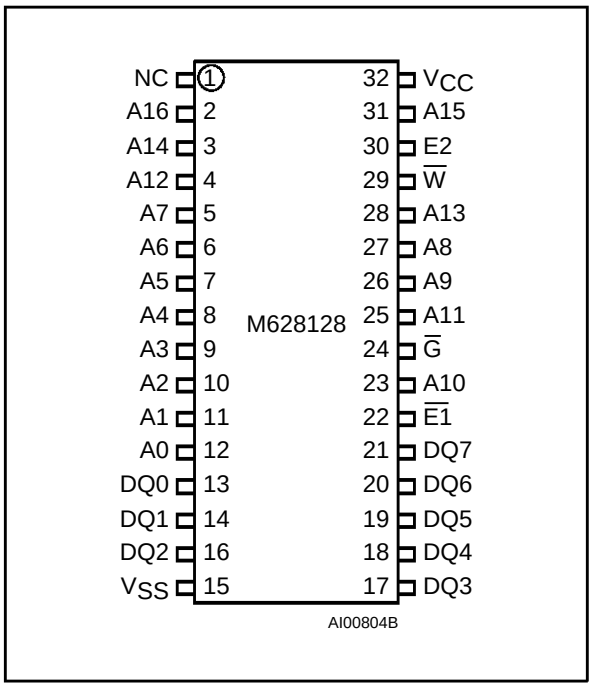
Notes: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Up to a maximum operating V_{CC} of 5.5V only.
3. One output at a time, not to exceed 1 second duration.

Table 3. Operating Modes

Mode	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0-DQ7	Power
Read	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IH}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	X	Hi-Z	Standby
Deselect	X	V_{IL}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

Figure 2. SOJ Pin Connections



Warning: NC = Not Connected.

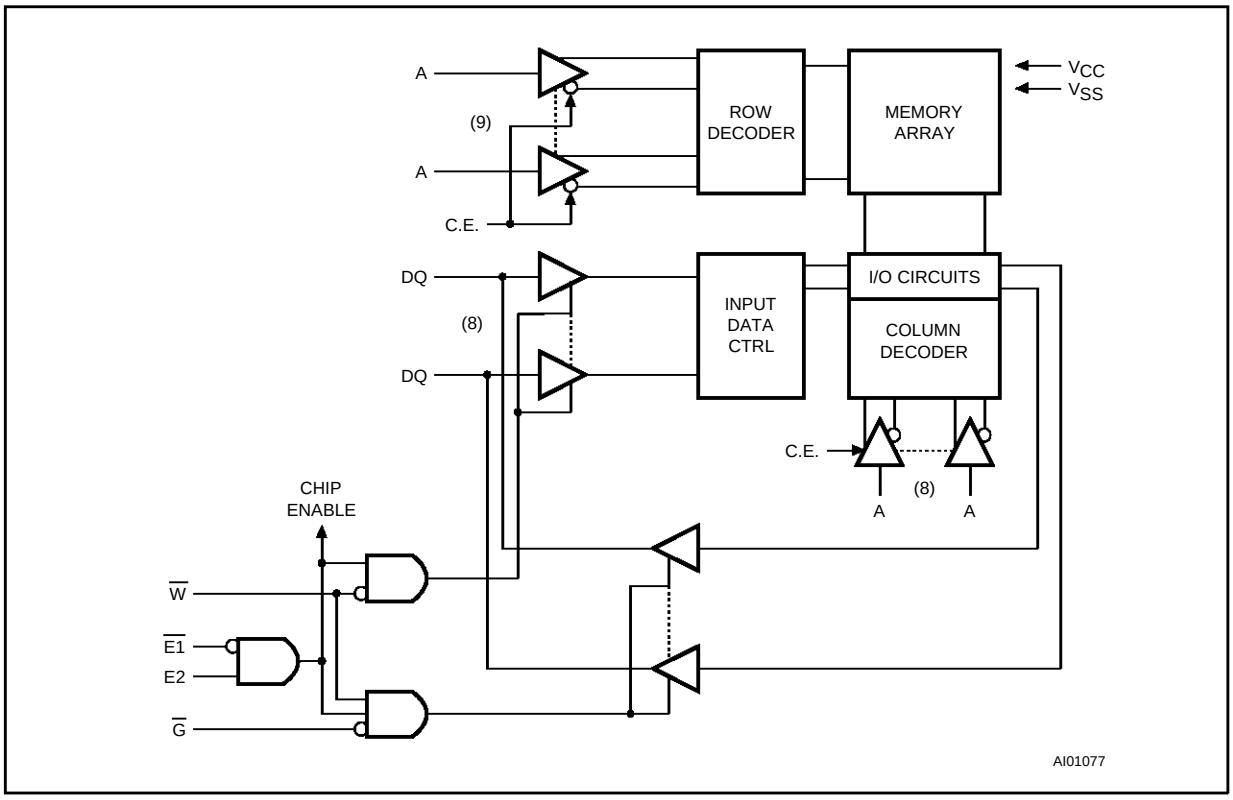
READ MODE

The M628128 is in the Read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and both Chip Enables ($\overline{E1}$ and E2) are asserted. This provides access to data from eight of the 1,048,576 locations in the static memory array, specified by the 17 address inputs. Valid data will be available at the eight output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low, $\overline{E1}$ is Low and E2 is High. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The M628128 is in the Write mode whenever the $\overline{W}$ and $\overline{E1}$ pins are Low, with E2 High. Either the Chip Enable inputs ($\overline{E1}$ and E2) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of both Chip Enables being active with $\overline{W}$ low. Therefore, address setup time is referenced to Write Enable and both Chip

Figure 3. Block Diagram



WRITE MODE (cont'd)

Enables as t_{AVWL}, t_{AVE1L} and t_{AVE2H} respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$, $\overline{W}$, or the falling edge of E2.

If the Output is enabled ($\overline{E1}$ = Low, E2 = High and $\overline{G}$ = Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVE1H} before the rising edge of $\overline{E1}$ or for t_{DVE2L} before the falling edge of E2, whichever occurs first, and remain valid for t_{WHDX}, t_{E1HDX} or t_{E2LDX}.

OPERATIONAL MODE

The M628128 has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E1}$ = High or E2 = Low). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{E1}$, and E2 as summarized in the Operating Modes table.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 1.5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

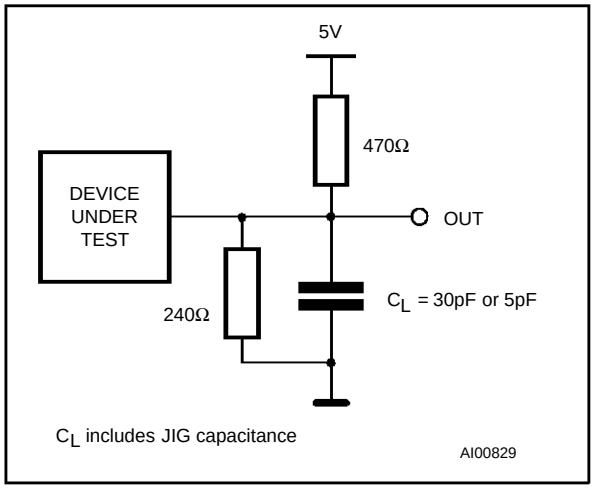


Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		8	pF
C_{OUT} (2)	Output Capacitance	V_{OUT} = 0V		8	pF

Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70 °C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC1} (1)	Supply Current	V_{CC} = 5.5V, (-15)		175	mA
		V_{CC} = 5.5V, (-20)		140	mA
I_{CC2} (2)	Supply Current (Standby) TTL	V_{CC} = 5.5V, $\overline{E1}$ = V_{IH} or E2 = V_{IL}, f = 0		30	mA
I_{CC3} (3)	Supply Current (Standby) CMOS	V_{CC} = 5.5V, $\overline{E1}$ ≥ V_{CC} – 0.2V or E2 ≤ 0.2V, f = 0		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4		V

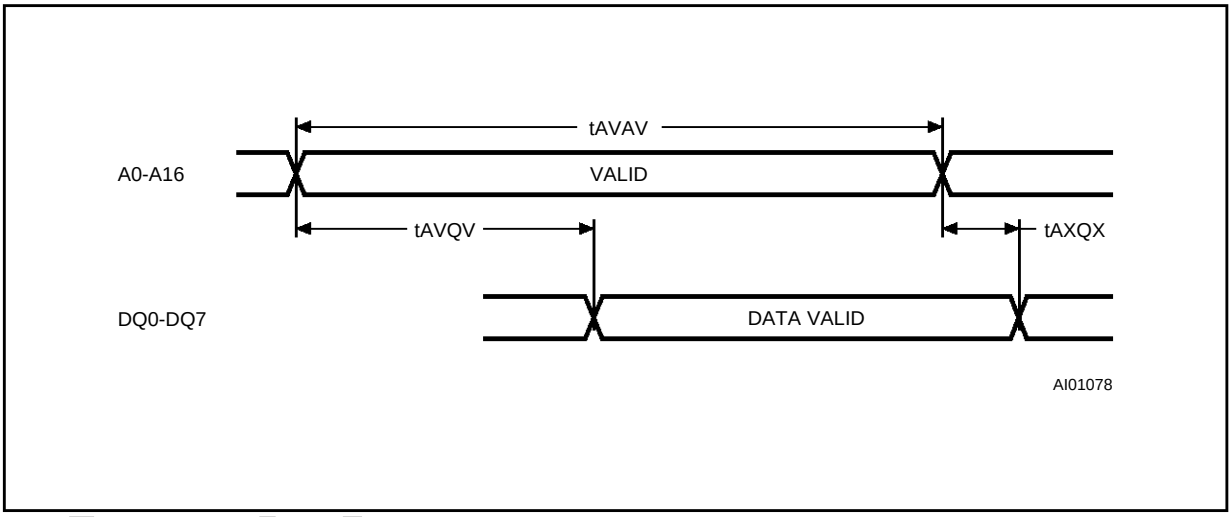
Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
2. All other Inputs at V_{IL} ≤ 0.8V or V_{IH} ≥ 2.2V
3. All other Inputs at V_{IL} ≤ 0.2V or V_{IH} ≥ V_{CC} – 0.2V

Table 6. Read and Standby Modes AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 5V ± 10%)

Symbol	Parameter	M628128				Unit
		-15		-20		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	15		20		ns
t_{AVQV} (1)	Address Valid to Output Valid		15		20	ns
t_{E1LQV} (1)	Chip Enable 1 Low to Output Valid		15		20	ns
t_{E2HQV} (1)	Chip Enable 2 High to Output Valid		15		20	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		7		8	ns
t_{E1LQX} (2)	Chip Enable 1 Low to Output Transition	2		2		ns
t_{E2HQX}	Chip Enable 2 High to Output Transition	2		2		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		ns
t_{E1HQZ} (2)	Chip Enable 1 High to Output Hi-Z	0	8	0	10	ns
t_{E2LQZ} (2)	Chip Enable 2 Low to Output Hi-Z	0	8	0	10	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z	0	7	0	9	ns
t_{AXQX} (1)	Address Transition to Output Transition	3		3		ns
t_{PU} (3)	Chip Enable 1 Low or Chip Enable 2 High to Power Up	0		0		ns
t_{PD} (3)	Chip Enable 1 High or Chip Enable 2 Low to Power Down		15		20	ns

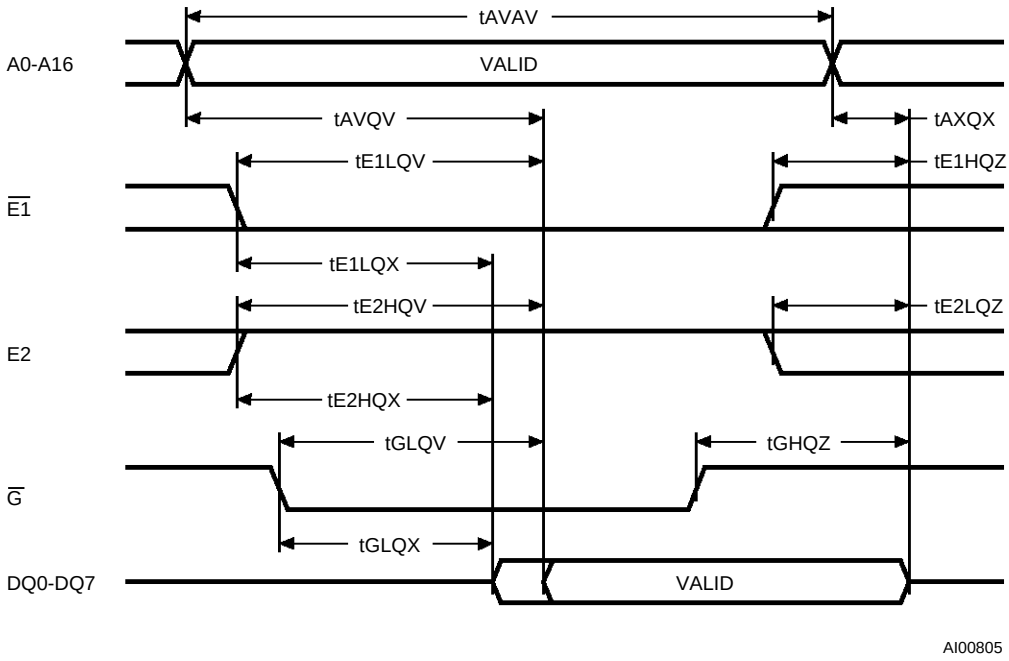
Notes: 1. C_L = 30pF (see Figure 4)
2. C_L = 5pF (see Figure 4)
3. Guaranteed but not tested (see Figure 7)

Figure 5. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E1}$ = Low, E2 = High, $\overline{G}$ = Low, $\overline{W}$ = High

Figure 6. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High

Figure 7. Standby Mode AC Waveforms

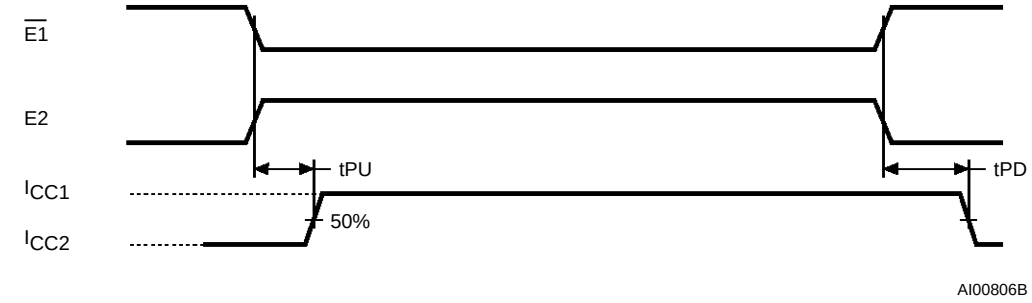
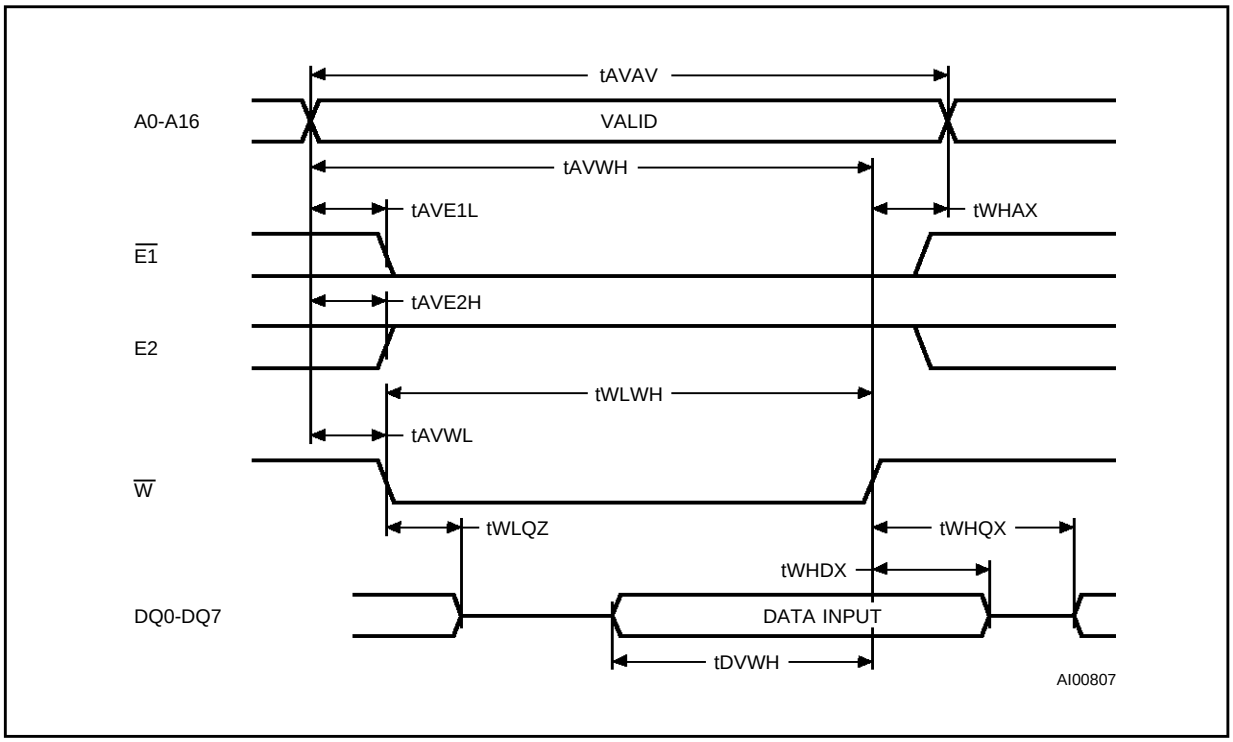


Table 7. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 5V ± 10%)

Symbol	Parameter	M628128				Unit
		-15		-20		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	15		20		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVWH}	Address Valid to Write Enable High	10		12		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	11		12		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	11		12		ns
t_{WLWH}	Write Enable Pulse Width	10		12		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	0		0		ns
t_{WLQZ} (1)	Write Enable Low to Output Hi-Z	0	8	0	10	ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		0		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	11		12		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	11		12		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	0		0		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	0		0		ns
t_{DVWH}	Input Valid to Write Enable High	8		12		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	8		12		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	8		12		ns

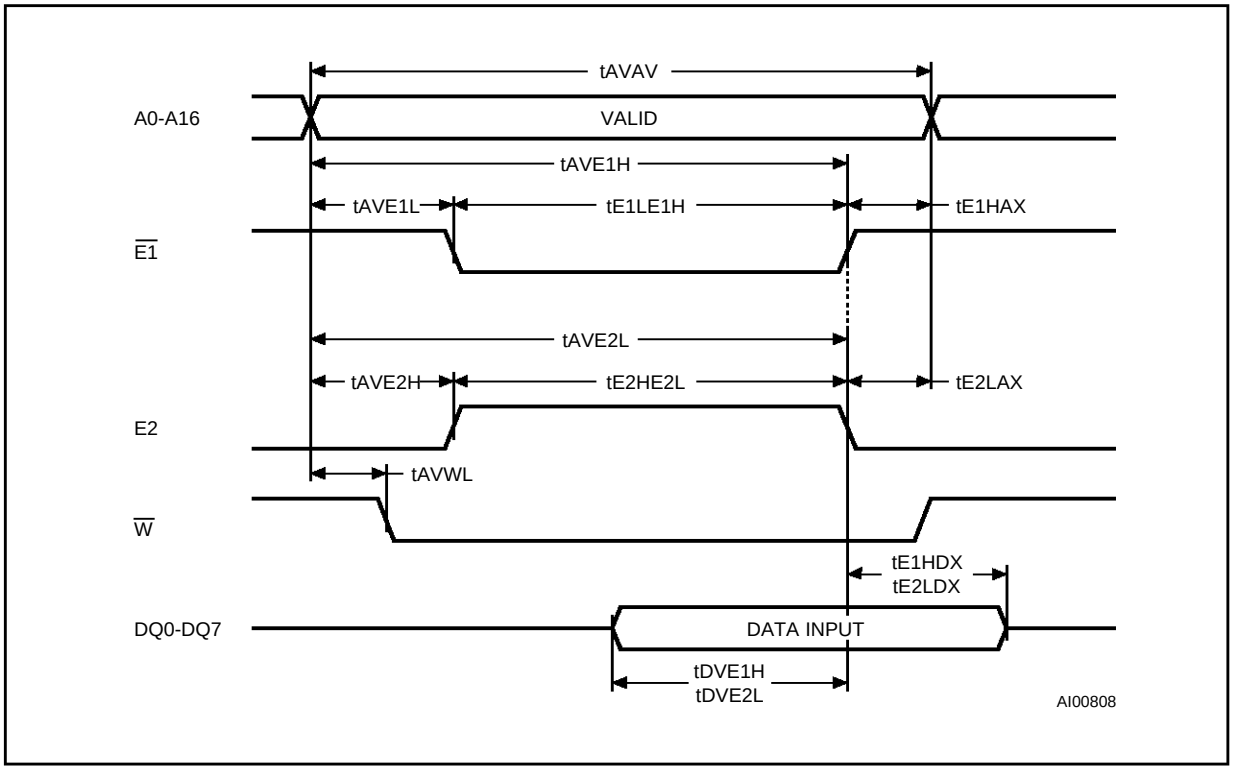
Note: 1. C_L = 5pF (see Figure 4)

Figure 8. Write Enable Controlled, Write AC Waveforms



Note: Output Enable ($\overline{G}$) = Low

Figure 9. Chip Enable Controlled, Write AC Waveforms



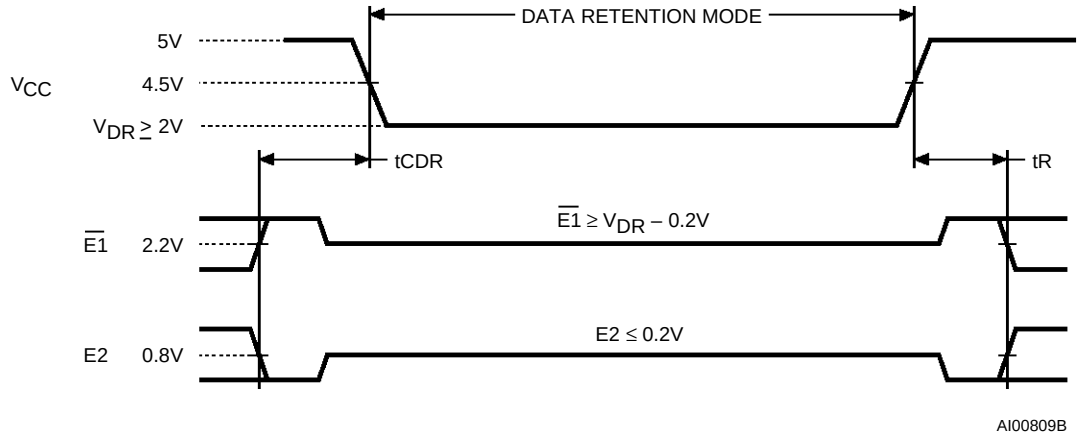
Note: Output Enable ($\overline{G}$) = High

Table 8. Low V_{CC} Data Retention Characteristics
(T_A = 0 to 70°C; V_{CC} = 2V to 4.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{CCDR} (1)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E1} \geq V_{CC} - 0.2V$, $E2 \leq 0.2V$, f = 0		500	µA
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E1} \geq V_{CC} - 0.2V$, $E2 \leq 0.2V$, f = 0	2	4.5	V
t_{CDR} (1, 2)	Chip Disable to Power Down	$\overline{E1} \geq V_{CC} - 0.2V$, $E2 \leq 0.2V$, f = 0	0		ns
t_R (2)	Operation Recovery Time			t_{AVAV}	ns

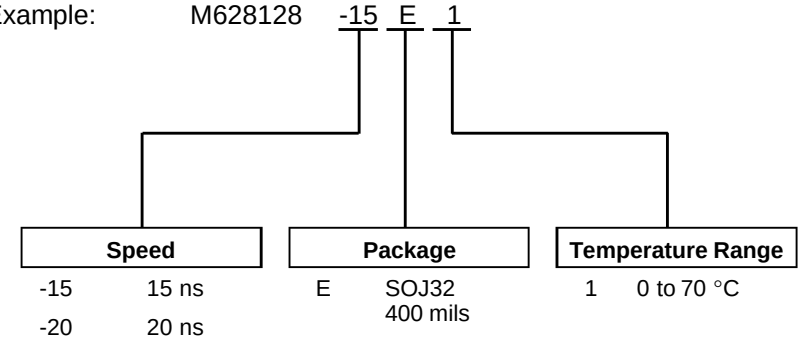
Notes: 1. All other Inputs $V_{IH} \geq V_{CC} - 0.2V$ or $V_{IL} \leq 0.2V$
2. See Figure 10 for measurement points. Guaranteed but not tested. t_{AVAV} is Read cycle time.

Figure 10. Low V_{CC} Data Retention AC Waveforms



ORDERING INFORMATION SCHEME

Example: M628128 -15 E 1

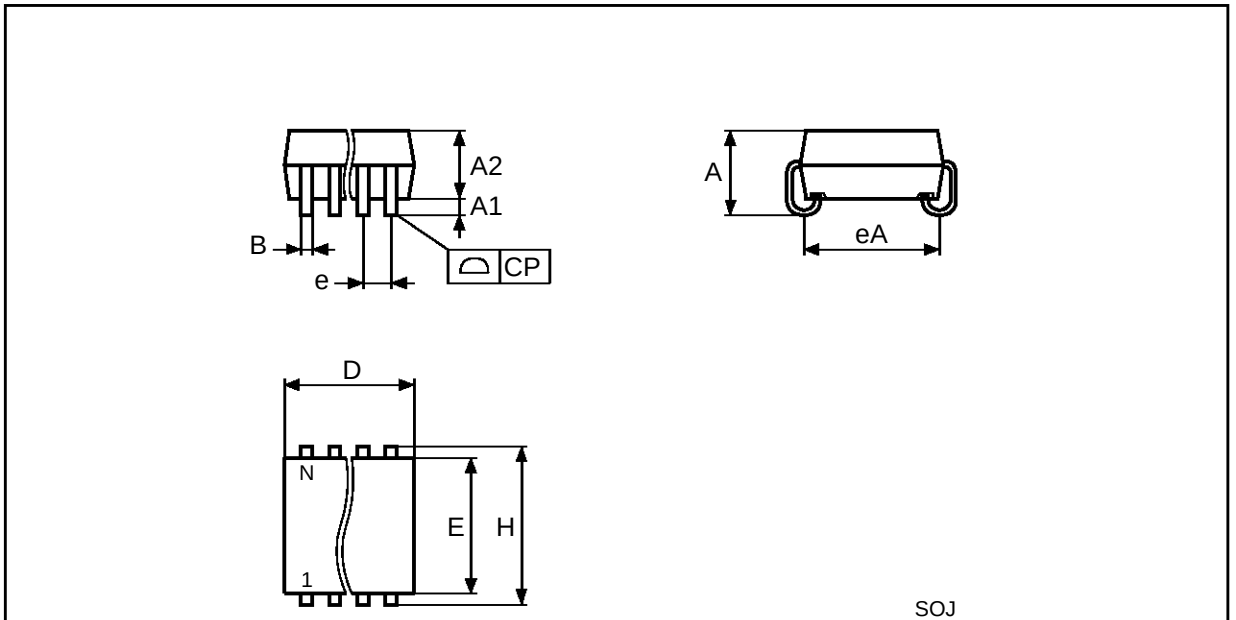


For a list of available options (Speed, Package, etc...) refer to the current Memory Shortform catalogue.
For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

SOJ32 - 32 lead Plastic Small Outline J-lead, 400 mils

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.33	3.68		0.131	0.145
A1		1.14	1.40		0.045	0.055
A2		2.18	2.29		0.086	0.090
B		0.38	0.51		0.015	0.020
D		20.83	21.08		0.820	0.830
E		10.03	10.29		0.395	0.405
e	1.27	–	–	0.050	–	–
eA		9.14	9.65		0.360	0.380
H		11.05	11.30		0.435	0.445
N	32			32		
CP			0.10			0.004

SOJ32



SOJ

Drawing is not to scale